ABSTRACT

A method of integrating the fabrication of a capacitor cell and a logic device region, wherein the surface area of a capacitor region is increased, and the risk of a capacitor depletion phenomena is reduced, has been developed. After formation of insulator filled STI regions featuring tapered sides, a portion of the insulator layer in an STI region is recessed below the top surface of the semiconductor substrate exposing a bare, tapered side of the semiconductor substrate. Ion implantation into the tapered side of the portion of semiconductor substrate exposed in the recessed STI portion, as well as into a top portion of semiconductor substrate located adjacent to the recessed STI portion, results in formation of a capacitor region now greater in surface area than a counterpart capacitor region which is formed via implantation into only a top portion of semiconductor substrate. Growth of a gate insulator layer and definition of gate structures in the logic device region, also simultaneously forms a capacitor dielectric layer on the underlying capacitor region, as well as a capacitor plate structure in the capacitor cell region.